In the Claims:

Please amend Claim 1 as follows.

1. (Three Times Amended) A data processing system comprising:

a communication bus;

a ~~master state~~ plurality of data processing ~~unit~~ units, the data processing units including:

~~a communication bus, the master state data processing unit exchanging asynchronous transfer mode protocol signals with the bus; and~~

~~at least one slave state data processing unit, the slave state data processing unit including:~~

a central processing unit;

a direct memory access unit coupled to the central processing unit, and

a Utopia mode interface unit coupled to the direct memory access unit, the Utopia interface unit acting in a receive mode and in a transmit mode; the Utopia transfer mode interface unit having:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals therewith; and

a buffer memory unit, the buffer memory unit buffering data signals between the direct memory access unit and the processor, ~~wherein the transfer of data cells between the buffer memory unit and the direct memory interface unit is determined by an event signal, the event signal indicating to the direct memory access unit that a data cell is stored in the buffer memory unit in the receive mode, the event signal indicating to the direct memory access unit that space for a data cell is available in buffer memory unit in the transmit mode~~;

wherein one of the data processing units operates in a master mode and the remainder of the data processing units operate in a slave mode.

2. (Previously Cancelled) ~~The data processing system as recited in claim 1 wherein the Utopia interface unit can act in a receive mode and in a transmit mode.~~

3. (Original) The data processing system as recited in claim 1 wherein the buffer memory unit is a first-in/first-out memory unit.

4. (Original) The data processing system as recited in claim 1 wherein the processor includes:

an input interface unit; and

an output interface unit; and wherein the buffer memory unit includes:

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

5. (Original) The data processing system as recited in claim 4 wherein data is transferred from the communication bus to the input buffer memory unit, and wherein data is transferred from the output buffer memory unit to the communication unit through the output interface unit.

6. (Original) The data processing system as recited in claim 5 wherein in the input buffer memory unit and the output buffer memory units are first-in/first-out memory units.

7. (Original) The data processing system as recited in claim 4 wherein the receive event signal is generated when the buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the buffer memory unit has space

for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the buffer memory unit from the direct memory access unit is begun.

Please amend Claim 8 as follows.

8. (Three Times Amended) A data processing system ~~comprising:~~ including ~~at least one slave state data processing unit;~~ a communication bus ~~the master state data processing unit~~ for exchanging asynchronous transfer mode protocol signals, ~~with the bus;~~ and a ~~master state~~ plurality of data processing ~~unit~~ units, the ~~master state~~ data processing ~~unit including~~ units having:

a central processing unit;

a direct memory access unit coupled to the central processing unit, and

a Utopia interface unit coupled ~~to~~ between the direct memory access unit; the Utopia interface unit ~~having~~ comprising:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals therewith; and

a buffer memory unit, the buffer memory unit buffering data signals between the direct memory access unit and the processor, an event signal indicating to the direct memory access unit when a data cell has been

received by the buffer memory unit in a receive mode, an event signal indicating to the direct memory access unit that space for a data cell is available in the receive mode;

wherein the UTOPIA interface unit can send and receive signals in either the master-mode or the slave-mode.

9. (Original) The data processing system as recited in claim 8 wherein the processor includes:

an input interface unit; and

an output interface unit: and wherein the buffer memory unit includes;

an input buffer memory unit; and

an output buffer memory unit.

10. (Original) The data processing system as recited in claim 9 wherein the data is transferred from the communication bus through the input interface unit to the input buffer memory unit, and wherein data is transferred from the output buffer memory unit through the output interface unit to the communication bus.

11. (Original) The data processing system as recited in claim 10 wherein the input buffer memory unit

and the output buffer memory unit are first-in/first-out memory units.

Please amend Claim 12 as follows:

12. (Twice Amended) An Utopia interface unit for providing an interface between an external data processing unit and a direct memory access unit, the interface unit comprising:

an input buffer memory unit, the input buffer memory unit providing data cells to the direct memory interface unit, the input buffer unit applying an event signal to direct memory access unit indicating that space is available for a data cell in a transmit mode, the ~~inp9ut~~ input buffer applying an event signal to the direct memory access unit indicating that data cell is stored therein in a receive mode;

an interface input unit, the interface input unit controlling the transmission of data cells from the external processing system to the input buffer memory unit;

an output buffer memory unit, the output buffer memory unit receiving data cells from the direct memory access unit; and

an interface output unit, the interface output unit controlling transmission of data cells from the output buffer memory unit to the external processing system;

wherein the interface unit can operate in either a master-mode or a slave mode with respect to the external data processing unit.

13. (Original) The interface unit as recited in claim 12 wherein the input buffer memory unit and the output buffer memory unit are first-in/first-out memory units.

14. (Original) The interface unit as recited in claim 12 wherein the first-in/first-out memory units can store at least two data cells.

15. (Original) The interface unit as recited in claim 12 wherein data from the input buffer memory unit is transferred to the direct memory access unit in response to word-read signal from the buffer memory unit.

16. (Original) The interface unit as recited in claim 12 wherein data from the direct memory unit is stored in the output buffer memory unit in response to a word-write signal from the output buffer memory unit.

17. (Original) The interface unit as recited in claim 12 wherein data is transferred from the external

processing unit to the input buffer unit in response to the cell-available signal from the input buffer unit.

18. (Original) The interface unit as recited in claim 12 wherein data is transferred from the output buffer memory unit to the external processing unit in response to the cell-available signal from the output buffer memory unit.

19. (Original) The interface unit as recited in claim 12 wherein the interface unit is operating in a slave mode, the transfer of data cells from the input buffer memory unit and the direct memory access unit being determined by a receive event signal, the transfer of data cells from the direct memory access unit to the output buffer memory unit being determined by a transmit event signal.

20. (Original) The data processing system as recited in claim 19 wherein the receive event signal is generated when the input buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the input buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the output buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of

the data cell to the output buffer memory unit from the direct memory access unit is begun.

Please cancel Claim 21.

21. (Currently Cancelled) ~~The data processing system as recited in claim 12 wherein the receive event signal is generated when the buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the buffer memory unit from the direct memory access unit is begun.~~

Please add Claim 22.

22. (Newly Added) The data processing system of claim 1 wherein the transfer of data cells between the buffer memory unit and the direct memory interface unit is determined by an event signal, the event signal indicating to the direct memory access unit that a data cell is stored in the buffer memory unit in the receive mode, the event signal indicating to the direct memory access unit that space for a data cell is available in buffer memory unit in the transmit mode.